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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,181	10/30/2000	Michael T. Moore	CY-0016	9600

7590

07/03/2002

Bradley T. Sako
3954 Loch Lomand Way
Livemore, CA 94550

EXAMINER

LIU, ANDREA

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/703,181

Applicant(s)

MOORE ET AL.

Examiner

Andrea Liu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-23 is/are allowed.
- 6) ☒ Claim(s) 1-6, 12 and 14 is/are rejected.
- 7) ☒ Claim(s) 7-11 and 13 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-3, 5, 6 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Borland U.S. Patent No. 6,219,824 B1.

The reference teaches the making of an integrated circuit that includes the limitations set forth in the claims. An integrated circuit is disclosed to include a programmable input/output process that allows the user to configure a plurality of circuits and a main functional unit to perform a predetermined data communication function (see abstract). Referring to claim 2, column 3 of the reference discloses the computer chip comprising signal lines that are operable to provide electrical communication via metal contacts and interconnects. Furthermore, a plurality of transistors mentioned make up the other part of the programmable portion, that of the

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logic gate. With reference to claim 3, the abstract also teaches a memory coupled to the communication portion of the integrated device, which in turn is coupled to the programmable logic itself, the memory also operating to store one or more of a plurality of configurations for the programmable logic. The reference then continues to teach a plurality of input/output pads coupled to the programmable logic, as stated in claim 5 of the application. Moreover, the reference shows the communication portion storing new configurations in the memory, and each of the plurality of configurations being operable to control a transmission of data to or from one or more of the plurality of input/output pads.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borland U.S. Patent No. 6,219,824 B1, as applied above, in view of Jefferson U.S. Patent No. 6,127,865.

The primary reference shows an integrated circuit device comprising programmable and communication portions, the programmable portion including a memory. However, it does not explicitly teach the generation of an internal clock signal that is phase shifted with respect to the clock signal.

The Jefferson reference discloses an integrated circuit programmable logic device wherein a first clock signal is provided as is a second clock signal that is a phase-shifted version

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of the first, shifted in phase by an amount which compensates for a logic signal delay (see column 3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include this component so as to effectively measure and manage delay and to reduce clock skew problems.

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borland U.S. Patent No. 6,219,824 B1 in view of Jefferson U.S. Patent No. 6,127,865, as applied above, and further in view of Reddy et al. U.S. Patent No. 5,942,914.

Together the references previously mentioned teach an integrated circuit device with a plurality of circuits configured by a user and able to perform data communication function aided by a timing circuit that reduces delay and clock skew problems. However, there has not been any clear teachings related to the presence of a data (MUX) multiplexer.

Reddy et al. teach a multiplexer, which is controlled by an array of programmable architectural bits so that the signals on selected global conductors can be routed to the inputs of selected logic modules (see column 1). Thus a data path may be established between one of a plurality of inputs and a data MUX output so as to meet the need to increase the logic density and overcoming the related obstacles consumption of a significant amount of the power used and the reduction of speed of production.

Thus one of ordinary skill in the art at the time the invention was made would have been motivated to modify the invention to include a multiplexer in order to provide flexibility of communications being performed by an integrated circuit since the number of connections would be reduced, allowing the functional logic density to increase properly.

Allowable Subject Matter

4. Claims 7-11 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims would be allowed based on the inclusion of the following step(s) involved in the making of an integrated circuit device containing programmable and communication portions which is/are not found in prior art –

Claim 7: Data operation circuits to include a block converter circuit in order to convert an input data word into an output data word having different bit values than the input data word.

Claim 8: The scrambler circuit in the data operation circuits to perform a scramble operation on the data received, which data may be represented by a scrambling polynomial.

Claim 9: The inclusion of an operation control store within the communication portion that provides operational values to the data operation circuits that controls the type of operation performed on the received data.

Claim 10: The data operation circuits with a scrambler circuit to perform the scrambling operation on the received data and the operation control store to provide operational values that represent at least one scrambling polynomial.

Claim 11: The operational control store to include circuits that will preset operational values based on the user operational value configured by a user.

Claim 13: The communication portion to include a physical layer circuit that provides a data output stream compatible with a particular data transmission media.

5. Claims 15-20 are allowable. The reason for allowance is based on the following limitations stated in the making of a semiconductor device which is/are not found in prior art –

Claim 15: The communication portion having non-programmable circuits designed to provide a selectable data communication function.

Claim 16: The communication portion to include a plurality of circuit blocks that each provides a different data communication function.

Claim 17: The communication portion to also include a selectable data path between each circuit block and a data output.

Claim 18: The presence of a block converter circuit and a scrambler circuit in the communication portion to encode input data words into output data words and to scramble data values according to an operational control value, respectively.

Claim 19: The inclusion of a block converted circuit and a de-scrambler circuit to de-scramble data values according to an operational control value in the communication portion of the semiconductor device.

Claim 20: The communication portion to include an operational control store that provides selectable operational control values to the scrambler circuit.

6. Claims 21-23 are allowable based on the below statements related to a method which is/are not found in prior art –

Claim 21: The performing of serial data communication functions on a communication portion of the integrated circuit that includes circuit blocks that are not synthesized.

Claim 22: The selecting of a polynomial value from a number of polynomial values and scrambling serial data according to the selected polynomial value.

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Claim 23: Performing serial data communication functions such as to encode the data having words of a first bit length into serial data having words of a second bit length that is different from the first bit length.

Conclusion

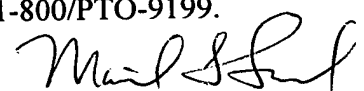
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Baxter U.S. Patent No. 5,815,405.
- b. Jones et al. U.S. Patent No. 5,815,510.
- c. Lawman U.S. Patent No. 5,946,478.
- d. Lawman et al. U.S. Patent No. 6,023,565.
- e. Raza U.S. Patent No. 5,943,488.
- f. Reddy et al. U.S. Patent No. 6,107,824.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrea Liu whose telephone number is (703) 305-4041. The examiner can normally be reached on 8:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 1-800/PTO-9199.


MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800